IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received February 10, 2021, accepted March 2, 2021, date of publication March 9, 2021, date of current version March 2, 2022.

Digital Object Identifier 10.1109/ACCESS.2021.3064715

Performance Evaluation of Seven Level Reduced Switch ANPC Inverter in Shunt Active Power Filter With RBFNN-Based Harmonic Current Generation

M. SIVASUBRAMANIAN, (Member, IEEE), C. S. BOOPATHI, (Member, IEEE), S. VIDYASAGAR, (Member, IEEE), V. KALYANASUNDARAM, AND SARAVANAN KALIYAPERUMAL, (Member, IEEE)

Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Chennai 603203, India

Corresponding author: Saravanan Kaliyaperumal (saravanank96@gmail.com)

ABSTRACT One of the serious issues that a Power System faces is the Power Quality (PQ) disturbance which occur mainly because of the non-linear loads. Among these PQ disturbances, harmonics play a vital role which should to be mitigated along with reactive power compensation. In this paper, a modified seven-level boost Active-Neutral-Point-Clamped (7LB-ANPC) inverter is utilized as a Shunt Active Power Filter (SAPF). Another vital aspect of this work is to retain the link voltage across the capacitor, which is accomplished through a PI controller tuned with an Adaptive Neuro-Fuzzy Inference System (ANFIS). An adaptive instantaneous p-q theory is instigated in the direction of extracting reference current and the harmonic extraction is carried out by using Radial Basis Function Neural Network (RBFNN). Gating sequence of inverter is generated for the outputs, which are attained from ANFIS and RBFNN and thus the opposite harmonics are injected to the Point of Common Coupling (PCC) by which current harmonics are eliminated with reactive power compensation. The 7Lb-ANPC inverter has a minimized number of switching devices with low switching losses and high boosting ability. By RBFNN based reference current generation, the source current THD of 0.89% is achieved. The proposed methodology is simulated through MATLAB and in hardware by utilizing FPGA Spartan 6E.

INDEX TERMS Power quality, shunt active power filter, multi-level inverters, active-neutral-point-clamped inverter, radial basis function neural network, adaptive neuro-fuzzy inference system.

I. INTRODUCTION

In power systems, there exist several disturbances, which have affected the quality of power in domestic and industrial applications it is primarily because of non-linear loads. Among various power quality (PQ) issues, harmonics, which are occurred in the system have interrupted the overall system's performance and these harmonics arise mainly because of the power electronic devices, SMPS, etc. and these are resolved by taking care of the source by which the problem arises [1]–[3]. FACTS devices are employed, by which the PQ problems like sag, swell, flickers, harmonics, and current imbalances are compensated [4].

To alleviate the current harmonics in the PCC, active or passive filters are employed and the passive filters are not preferred due to their fixed compensation and resonance. Hence there exist a need for a dynamic and flexible solution that paves the way for the development of active filters [5], [6]. Shunt active power filter (SAPF) is employed in this work and also in the works of literature review about SAPF. Alleviation of harmonics and power factor correction is carried out through the SAPF with cascade controller, which is discussed in [7]. In [8], a filter is designed through a 1φ transformer with a three-phase bridge, by which the harmonic current compensation is achieved. SAPF is designed with SRF controllers based on Park's transformation, by which the accurate reference current is generated for faster response, which is discussed in [9]. Series and shunt resonant problems are eliminated by the design of a hybrid filter for a four-wire three-phase system, which is discussed in [10]. To enhance the quality of voltage, a compensation technique is introduced for the optimal control of SAPF, which is presented in [11].

The associate editor coordinating the review of this manuscript and approving it for publication was Liu Hongchen.

In [12], SAPF is implemented to reduce the PQ problems, in which a control algorithm is implemented based on recursive inverse-based control. A modified recursive algorithm is introduced to control the gating sequence of the SAPF, by which the power quality problems are mitigated [13].

To reduce the harmonic content, a suitable power circuit has to be employed for the shunt active filters and a multi-level inverter (MLI) is the exact choice for this. Flying capacitor, diode clamped and cascaded H-bridge are the categories of MLI, which has more number of switches with the high cost and low efficiency. Also, these MLIs provide an increased number of voltage levels with low electro-magnetic interference and THD [14]–[16]. In this paper, modified seven-level boost active-neutral-point-clamped (7LB-ANPC) inverter is employed, by which the number of power electronic components are minimized without added capacitors and the literature shows some existing strategies. In [17], a simplified model is obtained by combining the dual T-type converters and 3-level diode neutral point clamped circuit, in which the capacitor voltage is also retained. A new strategy for seven-level ANPC is introduced in [18], in which the dynamic voltage balancing problem and the leaping of phase voltages are eliminated. A fusion of T-type converter and H-bridge is introduced in [19], in which space vector modulation is included to extend the modulation index that has been aimed for controlling the voltage of the floating capacitor. A topology with self-voltage balancing is introduced [20] to attain high voltage quality with a minimized count of switching devices. A more number of levels and improved the quality of power a cascaded type of multilevel inverter is proposed in [26] with reduced switching devices. 11 level is achieved by employed the 3 sources and 8 switches. More number of voltage levels are obtained with two different topologies and also it can be extended number of voltage source to obtain more levels with minimum switching devices [27].

The highest efficiency (98.5%) is achieved with the eight switches, triple voltage sources and obtained voltage level is 13. The detailed power loss analysis is done in [28]. A switched capacitor based 11 level voltage is generated in [29] with help of dual voltage source combined with 11 switches. And also to improve the performance of this topology a SHE-PWM technique is applied. By analogizing all the available 7L inverter topologies, here a modified seven-level inverter is presented, which limits the DC sources and the number of switches used and thus it minimizes the switching losses with high boosting capability.

The effective usage of shunt filter is realized only when a suitable theory is implemented for extracting the reference current. Here, an adaptive instantaneous p-q theory is realized in this work and the literature reviews have explained the application of various theories. Instantaneous reactive power theory and Fryze current extraction is analyzed at the generation of reference current, by which the harmonics are minimized and so the quality of power gets improved [21]. Reference currents are extracted through SRF theory, in which Park's transformation is employed for extracting the reference current and it results in a fast dynamic response [22]. The current harmonics, which have been generated on the load side are rectified by the shunt converter and also the shunt converter has rectified the PQ problems in the source side; and a control algorithm is realized for generating the reference signal [23].

Another major factor to be considered is the link voltage of the capacitor which has to be retained and this is realized by using the PI controller. In [24], PI controller is instigated to retain the capacitor voltage, which results in high switching frequency and low harmonic distortion. At [25], link voltage across the capacitor has been sustained with the use of the PI controller and a control algorithm is proposed for extracting the harmonics. In this work, this is attained with the tuned PI controller by using ANFIS, the performance of which is compared with that of the Fuzzy logic controller.

In this paper, harmonics mitigation is carried out by using a modified seven-level boost ANPC inverter, in which the extraction of reference current is carried out by using Radial Basis Function Neural Network (RBFNN) with adaptive instantaneous p-q theory. Also, the link voltage in the capacitor is retained by the PI controller and the parameters of PI controller are tuned with the Adaptive Neuro-Fuzzy Inference System (ANFIS), which is analogized with Fuzzy.

II. PROPOSED CONTROL METHODOLOGY

Non-linear loads like RL loads, RC loads, and DBR loads are generally included in distribution systems and so there arises harmonics in the source current. To get the optimal performance, an appropriate control methodology is proposed in this report, which is illustrated

In Figure 1 generally the source current (I_{sabc}) exhibits certain harmonics when associated with a non-linear load. With the help of by shunt active filter (SAPF), opposite current harmonics are injected in the PCC and a modified seven-level boost ANPC inverter is taken as the power circuit of SAPF. By this inverter, the number of switches and the switching losses is minimized with high boosting ability.

Moreover, the link voltage of the capacitor is also retained through the implementation of a PI controller tuned with ANFIS, which is compared with conventional PI and Fuzzy. Here, the reference current is generated by adaptive instantaneous p-q theory and the harmonics are extracted accurately by RBFNN. Thus the generated harmonics by RBFNN is fed to the PWM generator that has been incorporated with Hysteresis Current Controller (HCC), through which the required PWM pulses are generated for the proper working of the modified seven-level ANPC inverter. Thus the harmonics in the source current are eliminated by achieving reactive power compensation.

The modeling of the modified seven-level boost ANPC inverter, adaptive instantaneous p-q theory, RBFNN, voltage regulation of the capacitor are described elaborately in the upcoming sessions.

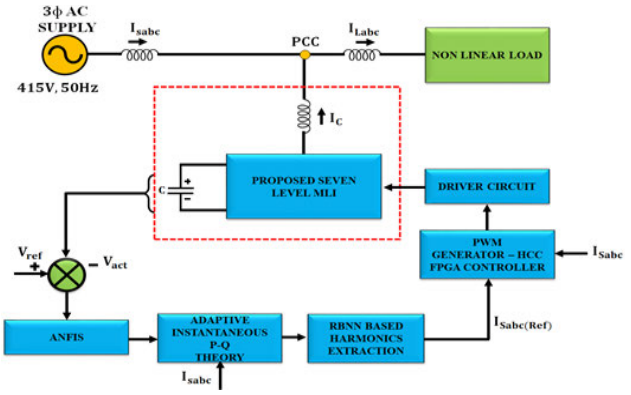


FIGURE 1. Proposed control methodology.

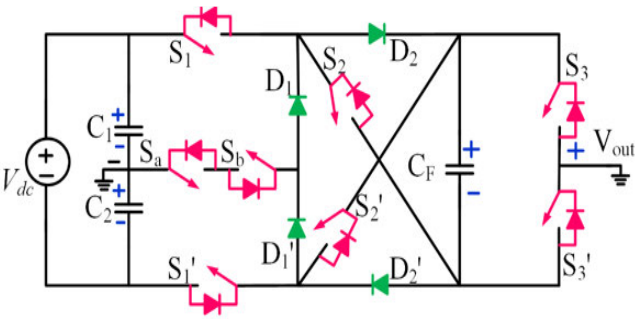


FIGURE 2. Proposed seven-level ANPC circuit Diagram.

III. MODELING OF THE PROPOSED CONTROL METHODOLOGY

A. A PROPOSED SEVEN LEVEL ACTIVE NEUTRAL POINT CLAMPED INVERTER TOPOLOGY

To enhance the ability and to balance the self-voltage of seven-level boost active neutral point clamped (7LB-ANPC) inverter, a modification is done, which includes the association of T-type neutral point clamped inverter along with the cross-coupled configuration of a capacitor. It is highly efficient as it has reduced the switching devices with minimized switching losses. This topology has a voltage-gain of 1.5 times greater than source voltage which is depicted in Figure 2 and it belongs to ANPC inverter topology.

The Modified APNC inverter includes a DC voltage source Vdc, floating capacitor C_F, eight switches namely S_1, S_2, S_3, S_1', S_2', S_3', Sa and Sb, also four diodes D_1, D_2, D_1', and D_2'. It has cross-linked switches and hybrid T- type inverter with dc capacitors that splits the input voltage into Vdc/2, which are coupled in parallel to the input dc source. One terminal of Sa and Sb is linked amidst D_1 and D_2, while the other terminal is connected at the midpoint of two capacitors. All the way through S_1, S1', D2 and D_2', a floating capacitor is paralleled to the dc capacitor. S_2 and S_2' are cross-connected amidst S_1, S1' and C_F. Table. I shows the switching sequence of developed topology, in which the outputs of voltage waveform are obtained by turning ON and OFF of switches and hence relying on such switching

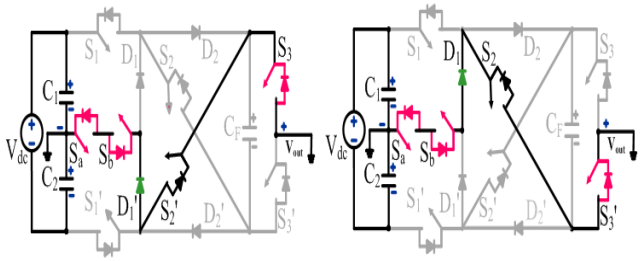


FIGURE 3. Mode 0 operation.

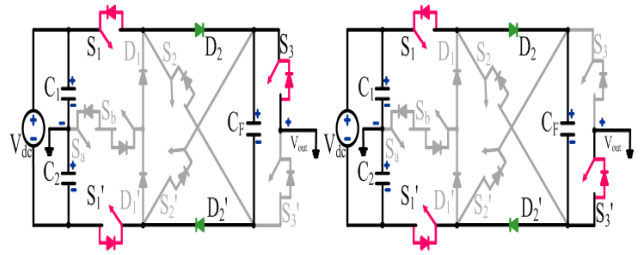


FIGURE 4. Mode 1 operation.

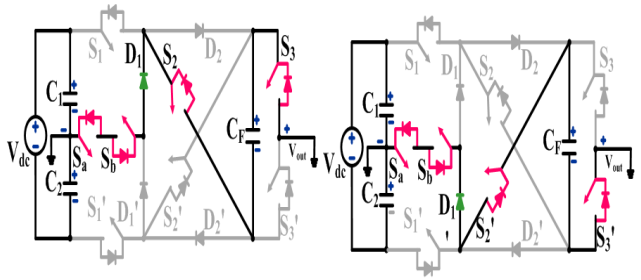


FIGURE 5. Mode 2 operation.

sequence capacitor voltage is sustained by the charging and discharging of capacitor.

Apart from S_a and S_b, all other switches have the maximum stress voltage V_{dc} and the stress voltage of S_a and S_b is given by half of the input voltage. The different operating modes of the 7LB-ANPC topology have been explained below.

1) MODE 0 (+ZERO,−ZERO)

Figure 3 depicts the operation of mode 0. In mode 0, continuous current flows from the source to load or from load to source at unity power factor by turning ON the switches D_1, S_3, S_2'/Sa, Sb, S_2, S_3' Also, it has less ON state switches, and the flow of current starts from Sa, Sb, D_1, S_3 or Sa, Sb, D_1' and S3'.

2) MODE 1 (+Vdc/2, −Vdc/2)

Figure 4 shows the operation of mode 1. In this mode, C_1 and C_2 are charged and so C_F is equivalent to the voltage source, therefore current flows through S_1, S_1', D_1 and D_1' which turns on S_3', S_3 to obtain $\pm V_{dc}/2$.

3) MODE 2 (+Vdc, −VDC)

Figure 5 depicts the operation of mode 2. The C_F voltage $+V_{dc}$ is transferred to load through Sa, Sb, S_2 and S_3. Here,

TABLE 1. Switching sequence seven- level ANPC topology.

V_{out}	S_1	S_2	S_3	S_1'	S_2'	S_3'	S_aS_b	Diodes	Status of CF
0	0	0	1	0	1	0	1	D_1&D_1'	-
	0	1	0	0	0	1	1	-	-
$+V_{dc}/2$	1	0	1	1	0	0	0	D_1&D_1'	Charging
$+V_{dc}$	0	1	1	0	0	0	1	-	discharging
$+3V_{dc}/2$	1	1	1	0	0	0	0	-	discharging
$-V_{dc}/2$	1	0	0	1	0	1	0	D_1&D_1'	charging
$-V_{dc}$	0	0	0	0	1	1	1	-	discharging
$-3V_{dc}/2$	0	0	0	1	1	1	0	-	discharging

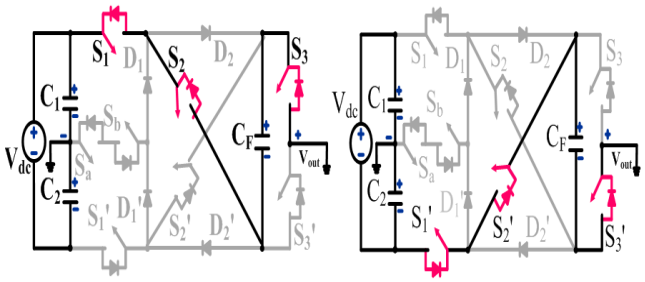


FIGURE 6. Mode 3 operation.

four ON switches are taken into account. As the two terminals of C_F is joined with the terminals of a diode, D_2 and D_2' are reverse biased.

4) MODE 3 (+3Vdc/2, −3Vdc/2)

Figure 6 depicts the operation of mode 3. By turning ON switches S_1, S_2 and S_3, the C_F voltage is summed with capacitor voltage which discharges 1.5 times voltage to load. As the two terminals of C_F is joined with the terminals of a diode, D_2 and D_2' are reverse biased.

In general, the output magnitudes of the existing topology are lower than the source voltage.

$$V_{omax} = 1/2\text{dc And } V_{orms} = 1/2\sqrt{2/4}\ \text{M Vdc} \quad (1)$$

Here, V_{omax} – Peak output voltage

Vo_{rms} – Voltage in RMS value

M - PWM modulation

The output voltage is halved to that of input naturally and so that the two capacitors maintain half the input voltage $V_{dc}/2$, also it is also self-balanced sustaining a voltage V_{dc}.

B. ADOPTIVE INSTANTANEOUS P-Q THEORY

This theory provides better precision and simple implementation but its drawback is that it cannot be used in unbalanced grid voltage. The computation of grid voltages to get fundamental balanced three-phase voltage components related to unbalanced voltages, a self-tuning filter is employed. To balance the issues SAPF's are modeled based mostly on P-Q Theory. In the beginning it is formed only for three-phase systems excluding neutral wire and then it is formed on behalf of three-phase four-wire system. This technique replaces three phases a-b-c into $\alpha - \beta$ and the theory is formed according to a set of rapid power already clear at a domain. So as for attaining active, reactive power components, with the aid of Clarke's transformation ($\alpha - \beta$), the three-phase voltages namely V_{sa}, V_{sb}, V_{sc} and the related currents I_a, I_b, I_c are transformed. Such transformation is noted as an outcrop of three-phase components into a fixed two-axis frame and the Clarke transformation related to voltage variables and current variables are represented as,

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_o \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} I_{s\alpha} \\ I_{s\beta} \\ I_{so} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} \quad (3)$$

The p (t) which is the instantaneous active power is represented as,

$$P(t) = V_{sa}I_{sa} + V_{sb}I_{sb} + V_{sc}I_{sc} \quad (4)$$

It can also be represented in a stationary frame as,

$$\begin{Bmatrix} P(t) = u_\alpha I_{s\alpha} + u_\beta I_{s\beta} \\ P_o(t) = u_o I_{so} \end{Bmatrix} \quad (5)$$

Here, P(t) represents the instantaneous active power, Po(t) represents the homopolar power sequence and also the representation of instantaneous reactive power is given as,

$$q(t) = 1/\sqrt{3}\,[(V_a - V_b)I_{sc} + (V_b - V_c)I_{sa} + (V_c - V_a)I_{sb} = V_\alpha I_{s\beta} - V_\beta)I_{s\alpha}] \quad (6)$$

The instantaneous reactive power q(t), defines higher than simple reactive power, and so all the voltage and current harmonics are taken into account while the habitual reactive power takes only the basics. The instantaneous active, reactive power components are represented in matrix-like,

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} \alpha & V_\beta \\ -V_\beta & V\alpha \end{bmatrix} \begin{bmatrix} I_{s\alpha} \\ I_{s\beta} \end{bmatrix} \quad (7)$$

Every single active and reactive power has a direct and an alternating component in which the former specifies the basics of current and voltage while the latter specifies the power of harmonics related to current and voltage. To extract harmonics from the source current, the direct term is isolated from the alternating component and for this purpose, a Low pass filter (LPF) is employed. After isolation of direct term from alternating components, the harmonic components related to source currents are expressed in terms of inverse equation and is given by,

$$\begin{bmatrix} I_{s\alpha} \\ I_{s\beta} \end{bmatrix} = 1/\,V_{s\alpha}^2 + V_{s\beta}^2 \begin{bmatrix} V_{s\alpha} & -V_{s\beta} \\ V_{s\beta} & V_{s\alpha} \end{bmatrix} \begin{bmatrix} \overline{p_s} \\ \overline{q_s} \end{bmatrix} \quad (8)$$

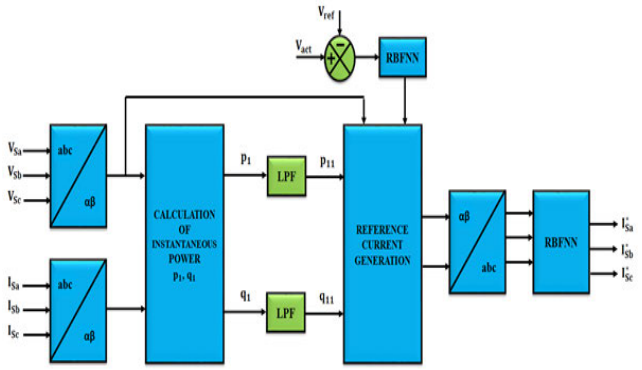


FIGURE 7. Adaptive Instantaneous p-q theory.

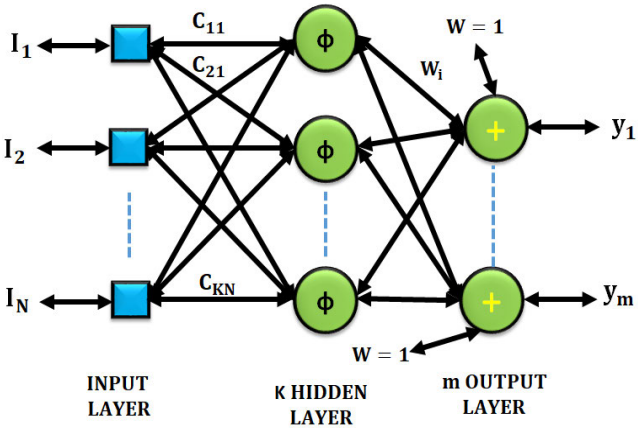


FIGURE 8. Representation of RBFNN.

Here, – represents the sign related to the alternating term and – represents the sign related to direct component of active, reactive power. Hence the reference current specifying SAPF given by,

$$\begin{bmatrix} I^*_{sa} \\ I^*_{sb} \\ I^*_{sc} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \bar{I}_{s\alpha} \\ \bar{I}_{s\beta} \end{bmatrix} \tag{9}$$

Figure 7 depicts the principle of active, reactive power and this method provides a benefit that there is a preference of compensating the harmonics and reactive power. In compensation to reactive power, power is directly applied towards the reference current and so the computation block precludes the usage of any extraction filter.

C. RADIAL BASIS FUNCTION NEURAL NETWORK (RBFNN)

To extract the harmonics accurately RBFNN is employed in this paper which is a feed-forward neural network comprising of input, hidden, and output layers. Fig 8 shows the representation of RBFNN in which the input layer with (I_1, $I_2 \ldots I_N$) inputs, hidden layer by K neurons, output layer with (Y_1, $Y_2 \ldots Y_N$) outputs are shown.

The input, hidden layers are connected by centers, and hidden, output layers are connected by weights.

The RBFNN can be represented as a Gaussian bias function.

$$\phi_i(x) = \exp\left[-\frac{(x - ci)^T(x - ci)}{2\sigma^2}\right], \quad i = 1, 2, \ldots K \tag{10}$$

where the output of the i^{th} *the* hidden layer is denoted as $\varphi i(x)$, the input data vector is denoted by x, the i^{th} hidden neuron's center is denoted by c_i, the normalization vector is denoted as σ_i then, A square vector of $(x\text{-}c_i$ signified like $(x\text{-}ci)^T$ $(x\text{-}c_i)$ and the output of node I (Yi) is also given as the linear weighted summation of the hidden and the output layers.

$$Y_i = W_i^T \phi(x), \quad i = 1, 2, \ldots m \tag{11}$$

where the output node's weight vector is represented as Wi and the vector representing the outputs from the hidden layer is denoted as $\phi(x)$.

1) TRAINING ALGORITHM-RBFNN

This is also known as the hybrid learning process which comprises two stages. The first stage is to locate the center for the radial bias function of the hidden neurons which is done through the Fuzzy K-means clustering algorithm. The second stage is to discover the weight between the hidden and the output layers which is done using a linear matrix inversion algorithm. The weight *w* is given as

$$W = A^{-1}\phi^T D \tag{12}$$

$$D = \begin{bmatrix} d(x_1) \\ d(x_2) \\ . \\ d(x_j) \\ . \\ d(x_i) \end{bmatrix} \tag{13}$$

where the desired output for l data samples is denoted by D, the output vector for $j^{th}{}_a$ sample is denoted by d (xj).

The matrix φ for l data samples and a variance matrix A^{-1} are represented as

$$\phi = \begin{bmatrix} \phi_1(x_1) & \phi_2(x_1) & \ldots\ldots & \phi_k(x_1) \\ \phi_1(x_2) & \phi_2(x_2) & \ldots\ldots & \phi_k(x_2) \\ . & . & \ldots\ldots & \\ . & . & \ldots\ldots & \\ \phi_1(x_l) & \phi_2(x_1) & \ldots\ldots & \phi_k(x_1) \end{bmatrix} \tag{14}$$

$$A^{-1} = \left[\phi^T \phi\right]^{-1} \tag{15}$$

This variance matrix A^{-1} needs negligible time for computation and so there is no need for iterations in the training phase.

2) HARMONIC EXTRACTION

The total harmonic extraction is carried out by incorporating the p-q theory with RBFNN. The first step is to create a delay buffer in which the sampling of data takes place at a constant rate and it is passed through the first-input first-output (FIFO) buffer by which a delayed vector of length N is created which is the same as the input vector of RBFNN. While creating the

FIFO buffer the first and the j[th] training sample is represented as x_1 and x_j and is given as

$$\phi_1 = \begin{bmatrix} p_{11} = p_1 \\ p_{21} = 0 \\ . \\ . \\ p_{N1} = 0 \end{bmatrix} \tag{16}$$

$$X_j = = \begin{bmatrix} p_{1j} & = p_j \\ p_{2j} & = p_{j-1} \\ . & . \quad \ldots \\ p_{Nj} & p_{j-N-1} \end{bmatrix} \tag{17}$$

$$X = [x_1 \ x_2 \ \ldots\ldots x_l] = \begin{bmatrix} p_{11} & p_{12} & \cdots\cdots & p_{1l} \\ p_{21} & p_{22} & \cdots\cdots & p_{2l} \\ . & . & \cdots\cdots & . \\ & . & \cdots\cdots & . \\ p_{N1} & p_{N2} & \cdots\cdots & p_{Nl} \end{bmatrix} \tag{18}$$

The matrix X for l training samples is given as

$$X = [x_1 \ x_2 \ \ldots\ldots x_l] = \begin{bmatrix} p_{11} & p_{12} & \cdots\cdots & p_{1l} \\ p_{21} & p_{22} & \cdots\cdots & p_{2l} \\ . & . & \cdots\cdots & . \\ & . & \cdots\cdots & . \\ p_{N1} & p_{N2} & \cdots\cdots & p_{Nl} \end{bmatrix} \tag{19}$$

The second step is to find the desired output in which the constant (DC) part of the active power is found through Fast Fourier Transform (FFT) for each x_j.

$$\mathrm{FFT}\left\{x_j\right\} = d_j^{DC} \tag{20}$$

As the number of the output node is one, only the DC part is considered and the desired output vector D obtained after applying FFT is given as

$$D = \begin{bmatrix} d_1^{DC} \\ \ldots \\ d_j^{DC} \\ \ldots \\ d_L^{DC} \end{bmatrix} \tag{21}$$

To find the center vectors (c_1, c_2,...c_k) Fuzzy K-means clustering algorithm is used and the Gaussian radial basis function is applied for finding φ of the outputs of the hidden neurons.

After attaining the RBFNN parameters i.e., centers and weights, in the RBFNN model, the embedded signal is sampled at the same rate in the training phase. Now the output is compared with the actual output and thus the oscillating part (harmonics) is easily removed.

D. REGULATION OF DC-LINK VOLTAGE USING PI, FUZZY AND ANFIS

Usually, the DC capacitor is employed in a circuit for two functions: a) in steady-state, where sustains voltage constant even with ripples, and b) in a transient state, where gives the power difference amidst load and the source. If the load changes then power also changes which charges or discharges the capacitor which further varies the reference source current as it is proportional to the capacitor voltage.

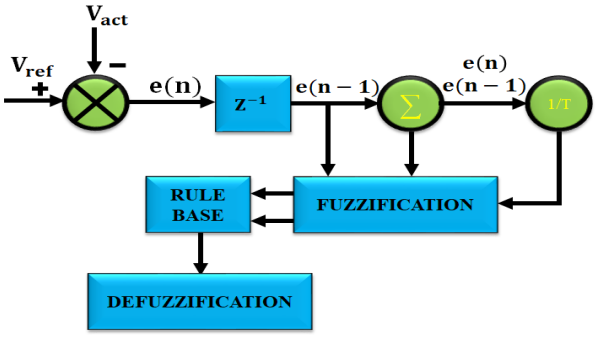


FIGURE 9. Fuzzy Logic Controller.

1) PI CONTROLLER

The PI controller helps maintain the link voltage and it is a widely used industrial application because of its simple design, easy construction, and low cost. Assume a feedback system, that design PI controller with a derivative time brought equivalent to zero so that the system function is given by,

$$K(s) = K(p)(1 + 1/(T(i)s)) \tag{22}$$

The response related to output relies on the integral of actuating signal and it is an error compensation method with the aid of a controller producing an output signal comprising of two parts among which one is proportional to actuating signal and the other one is proportional to its integral. It is used where ever speed is not taken into account.

2) FUZZY LOGIC CONTROLLER (FLC)

The FLC belongs to a multilevel-logic scheme whose variables involve its related membership function and it has three important components which are a) membership function degree alongside the vertical axis Y, b) related variables alongside horizontal axis X and c) vertical axis value related to the horizontal axis that are presented by the membership functions. The voltage at the capacitor that is equated by the aid of reference voltage then produces an error voltage e(n) and also variation at error e (n-1) which is taken as the input of Fuzzy logic controller. It includes the following processes. Figure 9 depicts the control scheme of FLC

a: FUZZIFICATION

It fuzzyfies crisp variables into linguistic variables. First, assume a value to the membership function which represents a value in the Y-axis. Among various membership functions, the triangular membership function which is the Mandeni type function is taken into account.

b: RULE BASIS

The reference current is generated relying on the rules of table error and the change in error.

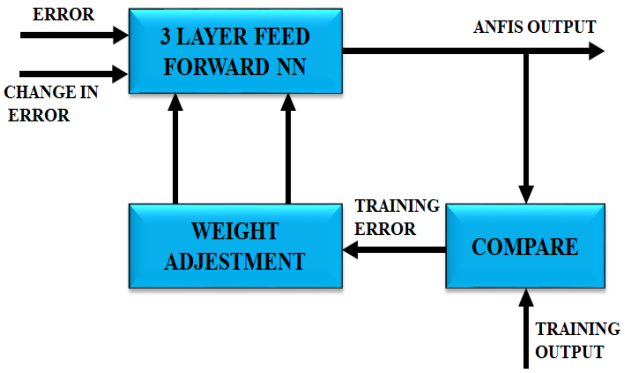


FIGURE 10. ANFIS controller.

E. DEFUZZIFICATION

It converts linguistic variables into crisp variables and so many types of methods are available for this type of conversion, in that COA (center of the area) is employed and a peak value of reference current is taken as the output of the fuzzy which is compared with the source current to produce pulses.

To bring out further improvement in the response of capacitor voltage regulation, an ANFIS controller is preferred

F. ANFIS CONTROLLER

To define the numerical and linguistic variables, ANFIS (Adaptive fuzzy neuro interference system) technique is preferred. Here, ANN is employed to tune the membership function while Fuzzy is employed to select the linguistic variables also Sugeno type function is preferred to model the ANFIS as it has a fixed or linear output. The firing strength z_i has the output as w_i for each rule. The rule describing the firing strength is given by

$$\text{Wi} = \text{AND}\,[F_1(x), F_2(x)] \tag{23}$$

Here, $F_1(x)$, $F_2(x)$ are the inputs regarding 1 and 2. The average of all the outputs yields the final output.

G. SAPF CONTROL USING ANFIS

To modify the membership function, neural networks are used and, a network is initially employed to fuzzify the crisp data, next to implement the rules, and then to defuzzify the crisp data. From the figure 10, the error along with a change of error is taken as inputs and the highest value of reference current, which has been employed for initiating SAPF is taken as the output.

Relying on the trained data, the output is generated and also many iterations are carried out to train the input data. Then a comparison is done amidst output data and ANFIS control data with training error, which requires an inspection procedure so as to avoid the over-fitting data. To model an ANFIS controller, the steps followed are given below,

Step 1:

Error with a range of values (−90, 90) and error change (−50, 50) then the step size is 0.5 which is taken as trained data.

TABLE 2. Source current THD values with different reference current extraction methods.

Harmonic current generation methods	% of THD Values
PQ Theory	4.5
SVM	3.9
ANN	3.2
CNN	2.1
RBFNN	0.89

Step 2:

Error with a range of values (−90, 90) and error change (−50, 50) then the step size is 1 which is taken as checking data.

ANFIS is produced with training error zero and also 1000 epochs are employed for training error and use 49 rules.

IV. RESULT AND DISCUSSIONS

Harmonics are produced in the source current due to usage of the non-linear loads. In this paper, mitigation of harmonics is achieved by the application of modified 7LB-ANPC by which opposite harmonics are introduced to the PCC. The dc-link voltage is controlled by ANFIS controller and the reference current is extracted based on adaptive instantaneous PQ theory while the harmonics are extracted based on RBFNN. This proposed methodology is verified using MATLAB/Simulink and the results were attained. The SAPF circuit and its control algorithm are designed from simple simulation blocks and executed in a discrete simulation environment to analyze steady-state as well as dynamic performance by system considering stable supply voltage of 415V, 50Hz. Meanwhile, a reference dc-link voltage of 100V is set across a 3300μF dc-link capacitor. A single inductance of 5mH is placed at the output of SAPF as a filter to eliminate the ripples, which are generated by the switching action of the SAPF. Instead of LC/LCL type filters, a simple L filter is introduced to reduce the overall complexity of the SAPF. A non-linear load, which comprises of uncontrolled diode-bridge rectifier that has been connected through the series combination of the resistor (50Ω) and an inductor (50mH) is considered as a source of harmonics.

Comparative analysis is performed for the benchmarked RBFNN based harmonic current generation method, ANFIS based dc-link voltage control with the existing harmonic current generation and dc-link voltage control algorithms.

The following simulation results have dictated the performance of the proposed adaptive instantaneous PQ theory-based reference current generation in detecting an essential harmonic component of source current for the given non-linear load. The below figures 11-17 show the steady-state simulated result for three-phase source voltage, load current, current injected at the PCC as well as source

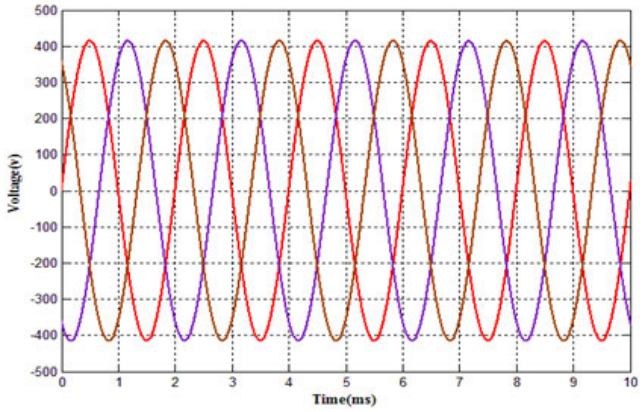


FIGURE 11. Source voltage waveform.

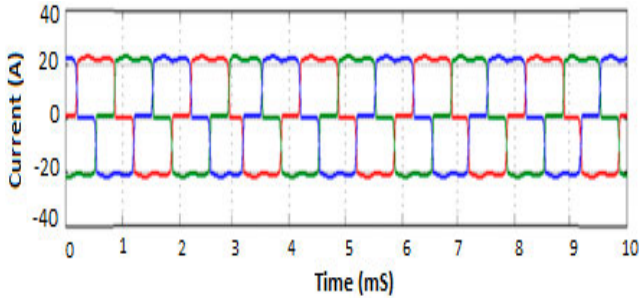


FIGURE 12. Load current waveform.

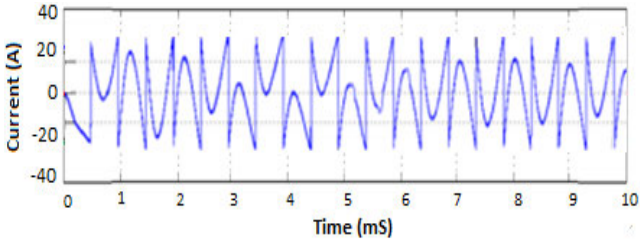


FIGURE 13. Current injected at the PCC.

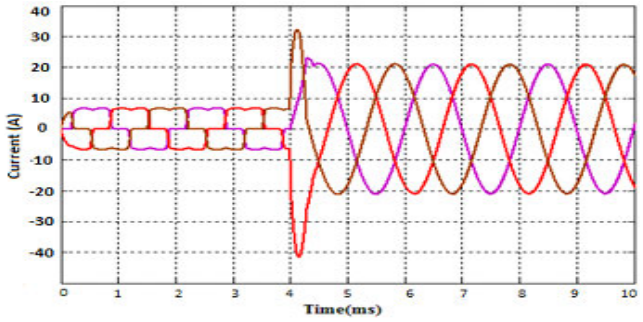


FIGURE 14. Source Current.

current for demonstrating a proposed algorithm's performance with non-linear inductive load.

Table 2 shows the THD values, which is obtained after applying SAPF with the existing harmonic generation methods. All the algorithms are found to be effective in maintaining the THD value within the limit.

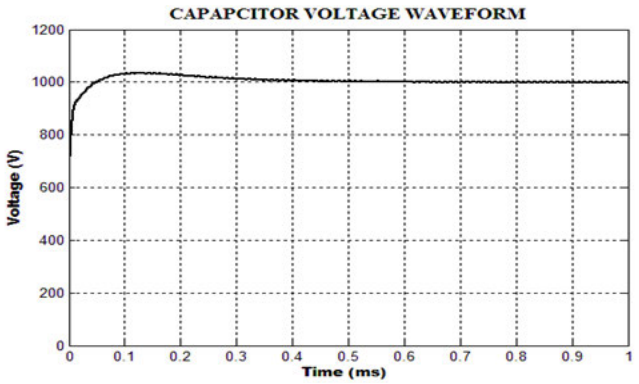


FIGURE 15. DC-link voltage.

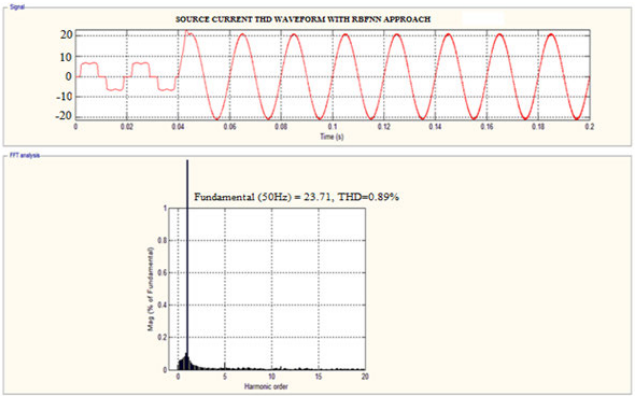


FIGURE 16. THD waveform with the RBFNN approach.

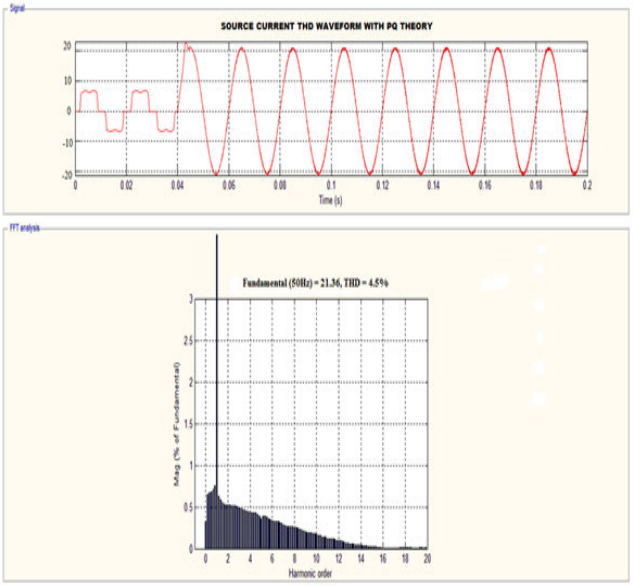


FIGURE 17. THD waveform with PQ theory.

From Figure.18, the proposed algorithm shows superior performance in mitigating the harmonic component from the source current by maintaining a lower THD value, which is linked with other approaches.

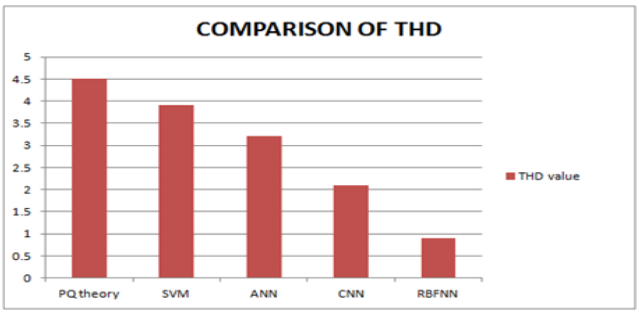


FIGURE 18. Comparison of harmonic current generation methods in terms of THD.

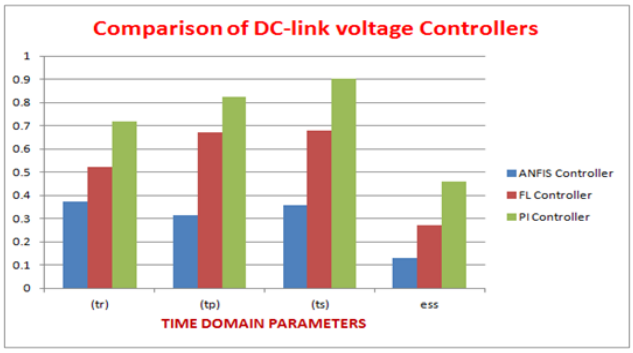


FIGURE 19. Comparison of DC-link voltage controllers.

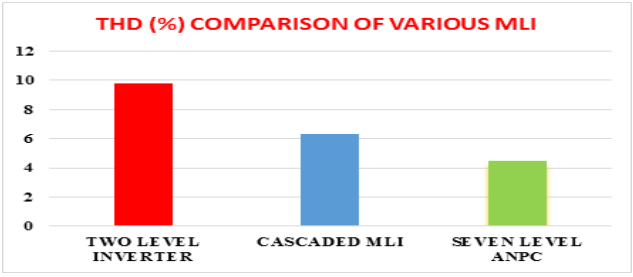


FIGURE 20. THD comparison of various MLI.

TABLE 3. Comparison of DC – link voltage controller.

Controller	Kp	Ki	(tr)	(tp)	(ts)	ess
ANFIS Controller	0.523	24.825	0.372	0.315	0.358	0.13
FUZZY LOGIC Controller	0.3618	13.2396	0.523	0.671	0.679	0.27
PI Controller	0.2794	9.7318	0.719	0.825	0.902	0.46

Further, the harmonic has eliminated the source current at in-phase through source voltage for a given non-linear load with maximum power factor.

In Table 3, the proposed ANFIS controller is found to respond quickly with a rise time of 0.3724s without much overshoots. It is observed that the existing algorithms have resulted in poor performance with high rise time.

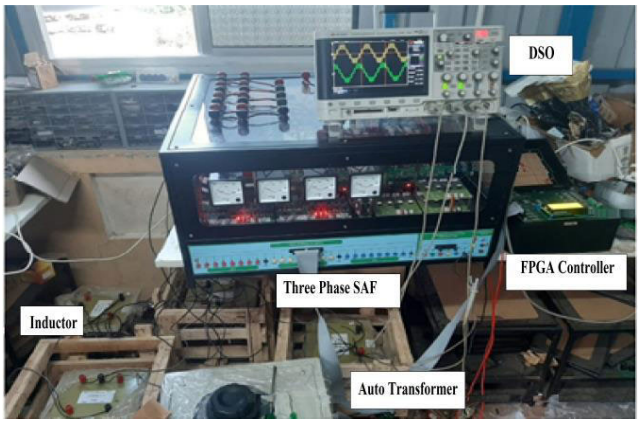


FIGURE 21. Experimental Setup.

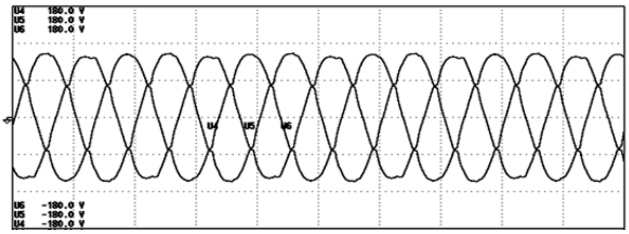


FIGURE 22. Source voltage waveform.

TABLE 4. Comparison of recently proposed 7L topologies with proposed topology.

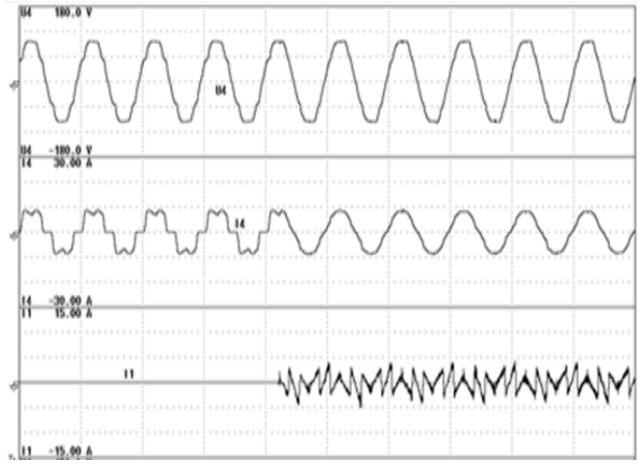
Topology	N_L	N_{swit}	N_{fc}	N_{sou}	N_{dio}	CF_{rating}	V_{gain}	TSV	MBV	F_{switch}
[19]	7	09	1	1	1	Vdc	1.5	4.7	2	2.5
[18]	7	12	2	1	-	Vdc/2	2.0	5.3	2	2.5
[27]	15	10	-	3	-	-	1.5	34	5	5.0
[28]	13	12	2	3	-	-	6.0	34	4	2.5
[29]	11	11	1	2	-	Vdc	1.25	21	5	2.5
Proposed Topology	**7**	**8**	**1**	**1**	**4**	**Vdc**	**1.5**	**4.7**	**1.5**	**2.5**

N_L= number of Levels $_z N_{Swit}$ = number of switches, N_{fc} = Number of floating capacitors, N_{sou} =number of dc voltage sources, N_{dio} =number of diodes, $C_{Frating}$= Floating capacitor voltage rating, ***TSV*** = Total standing voltage / unit, ***MBV*** = Maximum Blocking voltage / p.u, F_{swit} = Switching frequency in kHz.

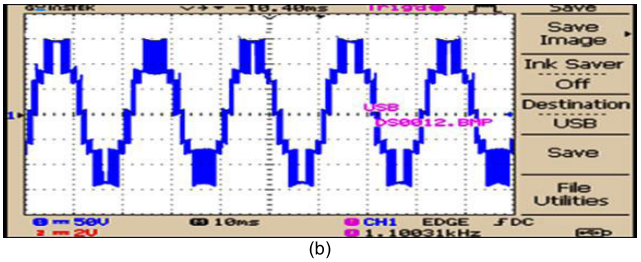
This projected algorithm requires a response time that is 50% less than the existing algorithms. Hence the dc-link voltages have regulated efficiently then a fixed voltage is maintained continuously, which has been shown in figure 19.

It is found that the RBFNN approach has not affect the performance of the ANFIS controller. These features make it worthier in implementing the proposed SAPF. Figure: 20 depicts the THD comparison of proposed seven-level ANPC with two-level inverter and cascaded MLI; and it is perceived that THD of 4.5% is attained for the proposed ANPC while the two-level inverter shows THD of 9.8% and the cascaded MLI shows a THD of 6.3%.

A detailed comparison of the modified 7LB- ANPC inverter with the recent single and cascaded sources topologies are carried out in table 4.



(a)



(b)

FIGURE 23. (a)Load voltage, Source current, RBFNN based SAPF compensation current. (b)Output voltage waveform of seven-level ANPC inverter.

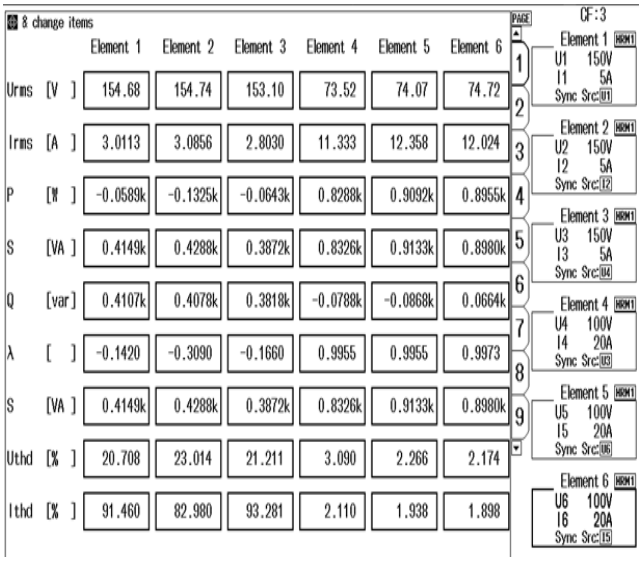


FIGURE 24. Three-phase load L-L and phase measurements.

The following parameters are considered i.e. Number of Levels N_L, Number of switches Nswit, capacitors Nfc, dc-sources N_{sou}, diodes N_{dio}, Floating capacitors rating $C_{Frating}$,, voltage-gain V_{gain}, total standing voltage TSV, Maximum blocking voltage MBV and operating frequency F_{swit}. From Table 4, it is perceived that the proposed topology requires minimum number of switches with minimized switching losses.

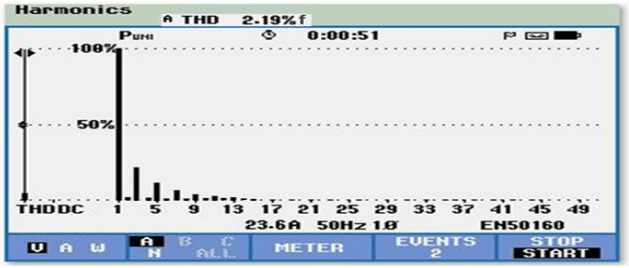


FIGURE 25. Source current THD value.

HARDWARE IMPLEMENTATION

SPECIFICATIONS

Input Power: 10 KW
Input voltage: 415V, 50 Hz
Source current: 24.09 A

VSI RATING

Input Power: 7KVA, 1000V, 50Hz
Autotransformer: 475V, 30A
Filter Inductance: 5mH (3-quantity)

NON LINEAR LOAD

R = 50ohm, 10A; Inductor: 50mH, Diode bridge rectifier

The proposed methodology is implemented in hardware by the Spartan 6 Field-Programmable Gate Array (FPGA) processor are shown in Figure.21. FPGA is considered as the apt and adequate technology which is employed in largely used applications. By this controller, PWM pulses have been generated for the inverter. The results are obtained through the CRO/Power quality analyzer for observing voltage and current waveforms.

Figure 22 and 23 (a-b) shows the voltage waveform of the seven-level ANPC inverter and it is observed that there are seven voltage levels and also compensation current injected to the system.

It is observed from the above figures 24 and 25 that the oscillations at current waveform are negated when SAPF is linked with 84ms and at the time, THD component in load current is 2.19%.

V. CONCLUSION

In this paper, harmonic mitigation and reactive power compensation are accomplished through a modified seven-level boost ANPC inverter, which exhibits high boosting ability with a minimized number of switches and low switching losses. The reference current generation is highlighted through the adaptive instantaneous p-q theory with RBFNN. Link voltage in the capacitor is retained by using ANFIS and which is compared by the PI controller and Fuzzy. PWM generator with a hysteresis current controller has generated the required gating sequence for the modified 7LB-ANPC inverter. A detailed comparison of modified 7LB-ANPC with the recent strategies has been carried out. The simulation results has highlighted that the proposed methodology is well suited for harmonic mitigation.

REFERENCES

[1] P. Harmonics, "Power system harmonics: An overview," *IEEE Trans. Power App. Syst.*, vol. PAS-102, no. 8, pp. 2455–2460, Aug. 1983, doi: 10.1109/TPAS.1983.317745.

[2] M. Rastogi, R. Naik, and N. Mohan, "A comparative evaluation of harmonic reduction techniques in three-phase utility interface of power electronic loads," *IEEE Trans. Ind. Appl.*, vol. 30, no. 5, pp. 1149–1155, Sep. 1994, doi: 10.1109/28.315225.

[3] R. Arnold, "Solutions to the power quality problem," *Power Eng. J.*, vol. 15, no. 2, pp. 65–73, Apr. 2001, doi: 10.1049/pe:20010202.

[4] D. Graovac, V. Katic, and A. Rufer, "Power quality problems compensation with universal power quality conditioning system," *IEEE Trans. Power Del.*, vol. 22, no. 2, pp. 968–976, Apr. 2007, doi: 10.1109/TPWRD.2006.883027.

[5] B. Singh, K. Al-Haddad, and A. Chandra, "A review of active filters for power quality improvement," *IEEE Trans. Ind. Electron.*, vol. 46, no. 5, pp. 960–971, Oct. 1999, doi: 10.1109/41.793345.

[6] M. El-Habrouk, M. K. Darwish, and P. Mehta, "Active power filters: A review," *IEE Proc.-Electr. Power Appl.*, vol. 147, no. 5, pp. 403–413, Sep. 2000.

[7] K. M. Tsang and W. L. Chan, "Design of single-phase active power filter using analogue cascade controller," *IEE Proc.-Electr. Power Appl.*, vol. 153, no. 5, pp. 735–741, Sep. 2006.

[8] G. A. de Almeida Carlos, C. B. Jacobina, J. P. R. A. Méllo, and E. C. D. Santos, "Shunt active power filter based on cascaded transformers coupled with three-phase bridge converters," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4673–4681, Sep. 2017, doi: 10.1109/TIA.2017.2702666.

[9] P. Salmerón and S. P. Litrán, "A control strategy for hybrid power filter to compensate four-wires three-phase systems," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1923–1931, Jul. 2010, doi: 10.1109/TPEL.2010.2043687.

[10] M. Badoni, B. Singh, and A. Singh, "Implementation of echo-state network-based control for power quality improvement," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5576–5584, Jul. 2017, doi: 10.1109/TIE.2017.2677359.

[11] H. Zhai, F. Zhuo, C. Zhu, H. Yi, Z. Wang, R. Tao, and T. Wei, "An optimal compensation method of shunt active power filters for system-wide voltage quality improvement," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1270–1281, Feb. 2020, doi: 10.1109/TIE.2019.2899561.

[12] M. Badoni, A. Singh, and B. Singh, "Adaptive recursive inverse-based control algorithm for shunt active power filter," *IET Power Electron.*, vol. 9, no. 5, pp. 1053–1064, Apr. 2016.

[13] P. Chittora, A. Singh, and M. Singh, "Gauss–Newton-based fast and simple recursive algorithm for compensation using shunt active power filter," *IET Gener., Transmiss. Distrib.*, vol. 11, no. 6, pp. 1521–1530, Apr. 2017.

[14] G.-J. Su, "Multilevel DC-link inverter," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 848–854, May 2005, doi: 10.1109/TIA.2005.847306.

[15] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010, doi: 10.1109/TIE.2010.2049719.

[16] H. Akagi, "Multilevel converters: Fundamental circuits and systems," *Proc. IEEE*, vol. 105, no. 11, pp. 2048–2065, Nov. 2017, doi: 10.1109/JPROC.2017.2682105.

[17] W. Li, J. Hu, S. Hu, H. Yang, H. Yang, and X. He, "Capacitor voltage balance control of five-level modular composited converter with hybrid space vector modulation," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5629–5640, Jul. 2018, doi: 10.1109/TPEL.2017.2740960.

[18] W. Sheng and Q. Ge, "A novel seven-level ANPC converter topology and its commutating strategies," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7496–7509, Sep. 2018, doi: 10.1109/TPEL.2017.2772885.

[19] H. Yu, B. Chen, W. Yao, and Z. Lu, "Hybrid seven-level converter based on T-type converter and H-bridge cascaded under SPWM and SVM," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 689–702, Jan. 2018, doi: 10.1109/TPEL.2017.2664068.

[20] M. Saeedian, M. E. Adabi, S. M. Hosseini, J. Adabi, and E. Pouresmaeil, "A novel step-up single source multilevel inverter: Topology, operating principle, and modulation," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3269–3282, Apr. 2019, doi: 10.1109/TPEL.2018.2848359.

[21] S. K. Chauhan, M. C. Shah, R. R. Tiwari, and P. N. Tekwani, "Analysis, design and digital implementation of a shunt active power filter with different schemes of reference current generation," *IET Power Electron.*, vol. 7, no. 3, pp. 627–639, Mar. 2014.

[22] A. Pigazo, V. M. Moreno, and E. J. Estébanez, "A recursive park transformation to improve the performance of synchronous reference frame controllers in shunt active power filters," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2065–2075, Sep. 2009, doi: 10.1109/TPEL.2009.2025335.

[23] A. Teke, L. Saribulut, and M. Tumay, "A novel reference signal generation method for power-quality improvement of unified power-quality conditioner," *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2205–2214, Oct. 2011, doi: 10.1109/TPWRD.2011.2141154.

[24] B.-R. Lin and T.-Y. Yang, "Three-level voltage-source inverter for shunt active filter," *IEE Proc.-Electr. Power Appl.*, vol. 151, no. 6, pp. 744 - 751, Nov. 2004.

[25] R. Dian, W. Xu, and C. Mu, "Improved negative sequence current detection and control strategy for H-bridge three-level active power filter," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 7, pp. 1–5, Oct. 2016, doi: 10.1109/TASC.2016.2602401.

[26] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 24498–24510, 2019, doi: 10.1109/Access.2019.2890872.

[27] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, "A new multilevel inverter topology with reduce switch count," *IEEE Access*, vol. 7, pp. 58584–58594, 2019, doi: 10.1109/ACCESS.2019.2914430.

[28] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, M. Tayyab, and M. K. Ansari, "Low switching frequency based asymmetrical multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 86374–86383, 2019, doi: 10.1109/ACCESS.2019.2925277.

[29] M. Rawa, M. D. Siddique, S. Mekhilef, N. M. Shah, H. Bassi, M. Seyedmahmoudian, B. Horan, and A. Stojcevski, "Dual input switched-capacitor-based single-phase hybrid boost multilevel inverter topology with reduced number of components," *IET Power Electron.*, vol. 13, no. 4, pp. 881–891, Mar. 2020.

M. SIVASUBRAMANIAN (Member, IEEE) was born in Salem, India, in 1978. He received the bachelor's degree in electrical and electronics engineering from Madras University, Chennai, in 2000, and the master's degree in power systems engineering from the College of Engineering, Guindy, Anna University, Chennai, in 2007. He is currently pursuing the Ph.D. degree with the SRM Institute of Science and Technology, India. His research interests include multilevel converters, DSTATCOM, electric vehicle, transformerless grid-connected systems, PV based charging stations, multilevel inverter fault analysis, and dc–dc converters for renewable energy application. He is also a Life Member of ISTE.

C. S. BOOPATHI (Member, IEEE) received the M.Eng. degree from Annamalai University, India, in 2001, and the Ph.D. degree from SRM University, India, in 2015. He joined the SRM Institute of Science and Technology as an Assistant Professor-II at the Department of Electrical and Electronics Engineering, Faculty of Engineering and Technology, in 2008, where he is currently working as an Associate Professor. He has more than 19 years of teaching experience. He has published and coauthored more than 41 articles in scientific journals. He has been the advisor of six Ph.D. and numerous post graduate students. He has been acting as a reviewer of many national and international journals. His research interests include electric vehicle, energy management control strategy, ANN, and particle swarm optimizations.

S. VIDYASAGAR (Member, IEEE) received the B.E. degree in electrical and electronics engineering from the University of Madras, in 2001, the M.E. degree in power systems from Anna University, in 2005, and the Ph.D. degree in feeder reconfiguration with DG placement in the distributed systems from the SRM Institute of Science and Technology, Chennai, India, in 2018. He is currently working as an Assistant Professor with the Department of Electrical and Electronics Engineering (EEE), Faculty of Engineering and Technology, College of Engineering and Technology, SRM Institute of Science and Technology. His research interests include power system operation and control, FACTS, power system protection renewable energy systems, energy storage technologies, and smart grids. He is also a Lifetime Member of ISTE and IEI.

V. KALYANASUNDARAM received the M.E. degree in power systems from Annamalai University, in 2005, and the Ph.D. degree in deregulated power systems from the SRM Institute of Science and Technology, Chennai, India. He is currently working as an Assistant Professor with the Department of Electrical and Electronics Engineering (EEE), SRM Institute of Science and Technology. His research interests include power system operation and control, optimal power flow, FACTS, and power system protection.

SARAVANAN KALIYAPERUMAL (Member, IEEE) received the B.E. degree in electrical and electronics engineering from the Alagappa Chettiar Government College of Engineering and Technology, Madurai Kamaraj University, India, in 1998, the M.E. degree in power electronics and drives from the College of Engineering, Guindy, Anna University, Chennai, India, in 2001, and the Ph.D. degree from JNTUK Kakinada, India, in 2018. He currently holds the post of an Associate Professor of Electrical and Electronics Engineering (EEE) with SRM IST. He has published several technical articles in national and international journals. His current research interests include renewable energy systems, electric vehicles, and multilevel inverters. He is also a Fellow Member of FIE, and a Life Member of ISTE and SESI.